IN THE CLAIMS:

Please amend claims 1 and 8-34, cancel claims 4-7 and add new claims 35-41 as follows:

1. (Currently Amended) An interface between a master device and a slave device, said interface comprising a ~~bit~~ serial data bidirectional signal line for conveying commands and associated data from said master device to said slave device, said ~~bit~~ serial data bidirectional signal line further conveying other signals, said other signals comprising a reset signal, an interrupt signal, and a learning sequence signal for specifying a duration of a bit time for data transferred from said slave device to said master device, where said interface comprises a resistance R coupled between the serial data bidirectional signal line and a circuit ground, and a pull up resistance R_{PU} installed in the master device, wherein R and R_{PU} together form a resistor voltage divider network.

2. (Original) An interface as in claim 1, where said master device is comprised of a personal digital assistant.

3. (Original) An interface as in claim 1, where said master device is comprised of a mobile terminal.

4. (Canceled)

5. (Canceled)

6. (Canceled)

7. (Canceled)

8. (Currently Amended) An interface as in claim 1, where said ~~bit~~ serial data bidirectional signal line further conveys a slave device connected/disconnected state to said master device.

9. (Currently Amended) An interface ~~circuit~~ for coupling a slave device to a master device, said interface [circuit] supporting a ~~bit~~ serial data bidirectional signal line that conveys commands and associated data from said master device to said slave device, said ~~bit~~ serial data bidirectional signal line further conveying other signals, said other signals comprising a reset signal, an interrupt signal, and a learning sequence signal for specifying a duration of a bit time for data transferred from said slave device to said master device, where said interface comprises, in said slave device, an Accessory Control Interface chip with an oscillator providing a clock signal to said Accessory Control Interface chip, where the bit time is a multiple of the clock signal, and where said master device adapts by sampling of the data transferred from said slave device in accordance with the specified duration of the bit time.

10. (Currently Amended) An interface ~~circuit~~ as in claim 9, where said interface ~~circuit~~ is disposed within said slave device and comprises an oscillator for generating a clock signal, where the bit time is a multiple of the clock signal period, and where said master device samples said ~~bit~~ serial data bidirectional signal line in accordance with the specified duration of the bit time.

11. (Currently Amended) An interface ~~circuit~~ as in claim 9, where said interface [circuit] is disposed within said slave device and comprises a non-volatile memory for storing slave device related feature data that is readable by said master device over said ~~bit~~ serial data bidirectional signal line in response to a read command sent from said master device to said interface ~~circuit~~ over said ~~bit~~ serial data bidirectional signal line.

12. (Currently Amended) An interface ~~circuit~~ as in claim 9, where said interface ~~circuit~~ is disposed within said slave device and comprises a challenge/response authentication function that is challenged in response to an authentication challenge command and associated challenge data received from said master device over said ~~bit~~ serial data bidirectional signal line, and where authentication result data is sent to said master device over said ~~bit~~ serial data bidirectional signal line in response to receiving an authentication result command from said master device over said ~~bit~~ serial data bidirectional signal line.

13. (Currently Amended) An interface ~~circuit~~ as in claim 9, where said ~~bit~~ serial data bidirectional signal line further conveys a slave device connected/disconnected state to said master device.

14. (Currently Amended) An interface ~~circuit~~ as in claim 9, where said master device is comprised of a mobile terminal.

15. (Currently Amended) An interface ~~circuit~~ as in claim 14, where said mobile terminal samples said ~~bit~~ serial data bidirectional signal line at a rate established by a mobile terminal sleep clock.

16. (Currently Amended) An interface ~~circuit~~ as in claim 9, where said master device is comprised of a personal digital assistant.

17. (Currently Amended) An interface ~~circuit~~ for coupling a slave device to a master device, said interface ~~circuit~~ being disposed in said slave device and supporting a ~~bit~~ serial data bidirectional signal line that conveys commands and associated data from said master device to said slave device, said ~~bit~~ serial data bidirectional signal line further conveying other signals, said other signals comprising a reset signal, where said interface comprises, in said slave device, an Accessory Control Interface chip with an oscillator providing a clock signal to said Accessory Control Interface chip, where the bit time is a multiple of the clock signal, and where said master device adapts by sampling of the data transferred from said slave device in accordance with the specified duration of the bit time.

18. (Currently Amended) An interface ~~circuit~~ as in claim 17, where said other signals further comprise an interrupt signal and a learning sequence signal for specifying a duration of a bit time for data transferred from said slave device to said master device.

19. (Currently Amended) An interface ~~circuit~~ for coupling a slave device to a master device, said interface ~~circuit~~ being disposed in said slave device and supporting a ~~bit~~ serial data bidirectional signal line that conveys commands and associated data from said master device to said slave device, said ~~bit~~ serial data bidirectional signal line further conveying

other signals, said other signals comprising an interrupt signal, where said interface comprises, in said slave device, an Accessory Control Interface chip with an oscillator providing a clock signal to said Accessory Control Interface chip, where the bit time is a multiple of the clock signal, and where said master device adapts by sampling of the data transferred from said slave device in accordance with the specified duration of the bit time.

20. (Currently Amended) An interface ~~circuit~~ as in claim 19, where said other signals further comprise a reset signal and a learning sequence signal for specifying a duration of a bit time for data transferred from said slave device to said master device.

21. (Currently Amended) An interface ~~circuit~~ for coupling a slave device to a master device, said interface ~~circuit~~ being disposed in said slave device and supporting a ~~bit~~ serial data bidirectional signal line that conveys commands and associated data from said master device to said slave device, said ~~bit~~ serial data bidirectional signal line further conveying other signals, said other signals comprising a learning sequence signal for specifying a duration of a bit time for data transferred from said slave device to said master device, where said interface comprises, in said slave device, an Accessory Control Interface chip with an oscillator providing a clock signal to said Accessory Control Interface chip, where the bit time is a multiple of the clock signal, and where said master device adapts by sampling of the data transferred from said slave device in accordance with the specified duration of the bit time.

22. (Currently Amended) An interface ~~circuit~~ as in claim 21, where said interface [circuit] comprises an oscillator for generating a clock signal, where the duration of the bit time is a multiple of the clock signal period, and where said master device samples said ~~bit~~ serial data bidirectional signal line in accordance with the specified duration of the bit time.

23. (Currently Amended) An interface ~~circuit~~ as in claim 22, where a logic zero and a logic one are distinguished by a presence or absence of a transition occurring on said ~~bit~~ serial data bidirectional signal line by a predetermined point in the specified duration of the bit time.

24. (Currently Amended) An interface ~~circuit~~ as in claim 23, where the specified duration of the bit time is given by T, and where the predetermined point is about T/2.

25. (Currently Amended) An interface ~~circuit~~ as in claim 21, where said interface ~~circuit~~ comprises at least one register that is readable by said master device over said ~~bit~~ serial data bidirectional signal line.

26. (Currently Amended) An interface ~~circuit~~ as in claim 21, where said interface ~~circuit~~ comprises at least one register that is writable by said master device over said ~~bit~~ serial data bidirectional signal line.

27. (Currently Amended) An interface ~~circuit~~ as in claim 21, where said interface ~~circuit~~ comprises at least one memory device location that is readable by said master device over said ~~bit~~ serial data bidirectional signal line.

28. (Currently Amended) An interface ~~circuit~~ as in claim 21, where said interface ~~circuit~~ comprises at least one memory device location that is writable by said master device over said ~~bit~~ serial data bidirectional signal line.

29. (Currently Amended) An interface ~~circuit~~ as in claim 21, where said interface ~~circuit~~ comprises an authentication block that is addressable by commands sent by said master device over said ~~bit~~ serial data bidirectional signal line, and that responds to at least one command with response data sent to said master device over said ~~bit~~ serial data bidirectional signal line.

30. (Currently Amended) An interface ~~circuit~~ as in claim 21, where said other signals further comprise a reset signal and an interrupt signal.

31. (Currently Amended) A ~~method for communicating between a~~ master device ~~and a slave device,~~ comprising:

~~coupling the~~ an interface for coupling to a slave device ~~to the master device through an interface~~, the interface comprising a ~~bit~~ serial data bidirectional signal line;

~~sending~~ wherein a reset signal is sent from the master device to the slave device over the ~~bit~~ serial data bidirectional signal line;

~~sending~~ and a learning sequence signal is sent to the master device over the ~~bit~~ serial data bidirectional signal line for specifying a duration of a bit time for data transferred between the master device and the slave device; ~~and~~

~~communicating~~ wherein at least one of data and commands are communicated between the master device and the slave device over the ~~bit~~ serial data bidirectional signal line, and the interface comprises an Accessory Control Interface chip with an oscillator providing a clock signal to said Accessory Control Interface chip, where the bit time is a multiple of the clock signal, and where said master device adapts by sampling of the data transferred from said slave device in accordance with the specified duration of the bit time.

32. (Currently Amended) ~~A method~~ The master device as in claim 31, where ~~communicating comprises~~ the master device ~~sampling~~ samples the ~~bit~~ serial data bidirectional signal line in accordance with the specified duration of the bit time.

33. (Currently Amended) ~~A method~~ The master device as in claim 32, where a logic zero and a logic one are distinguished by a presence or absence of a transition occurring on the ~~bit~~ serial data bidirectional signal line by a predetermined point in the specified duration of the bit time.

34. (Currently Amended) ~~A method~~ The master device as in claim 33, where the specified duration of the bit time is given by T, and where the predetermined point is about T/2.

35. (New) The master device as in claim 31, where the master device includes a mobile terminal.

36. (New) The master device as in claim 31, where the master device is selected from the group consisting of a cellular telephone, a personal computer, a personal organizer, a personal digital assistant, an email terminal, a laptop computer, a notebook computer, a workstation, and a home electronic device.

37. (New) A slave device comprising:

an interface for coupling to a master device, the interface comprising a serial data bidirectional signal line;

wherein a reset signal is sent from the master device to the slave device over the serial data bidirectional signal line; and

a learning sequence signal is sent to the master device over the serial data bidirectional signal line for specifying a duration of a bit time for data transferred between the master device and the slave device; wherein at least one of data and commands are communicated between the master device and the slave device over the serial data bidirectional signal line, and the interface comprises an Accessory Control Interface chip with an oscillator providing a clock signal to said Accessory Control Interface chip, where the bit time is a multiple of the clock signal, and where said master device adapts by sampling of the data transferred from said slave device in accordance with the specified duration of the bit time.

38. (New) The slave device as in claim 37, comprising an accessory selected from the group consisting of a battery charger, a headset and a hands free adapter.

39. (New) A master device for coupling to a slave device through an interface, the interface comprising a serial data bidirectional signal line for conveying commands and associated data from said master device to said slave device, said serial data bidirectional signal line further conveying other signals, said other signals comprising a reset signal, an interrupt signal, and a learning sequence signal for specifying a duration of a bit time for data transferred from said slave device to said master device, where said interface comprises a

resistance R coupled between the serial data bidirectional signal line and a circuit ground, and a pull up resistance R_{PU} installed in the master device, wherein R and R_{PU} together form a resistor voltage divider network.

40. (New) A slave device for coupling to a master device through an interface, the interface comprising a serial data bidirectional signal line for conveying commands and associated data from said master device to said slave device, said serial data bidirectional signal line further conveying other signals, said other signals comprising a reset signal, an interrupt signal, and a learning sequence signal for specifying a duration of a bit time for data transferred from said slave device to said master device, where said interface comprises a resistance R coupled between the serial data bidirectional signal line and a circuit ground, and a pull up resistance R_{PU} installed in the master device, wherein R and R_{PU} together form a resistor voltage divider network.

41. (New) A master device comprising:

an interface for coupling to a slave device, the interface comprising a serial data bidirectional signal line;

wherein a reset signal is sent from the master device to the slave device over the serial data bidirectional signal line; and

a learning sequence signal is sent to the master device over the serial data bidirectional signal line for specifying a duration of a bit time for data transferred between the master device and the slave device; wherein at least one of data and commands are communicated between the master device and the slave device over the serial data bidirectional signal line, and the interface comprises a resistance R coupled between the serial data bidirectional signal line and a circuit ground, and a pull up resistance R_{PU} installed in the master device, wherein R and R_{PU} together form a resistor voltage divider network, wherein presence of the resistance R affects the serial data bidirectional signal line to enable detection of a slave device connected/disconnected state.